

METHOD AND APPARATUS FOR TIMING CHARACTERIZATION OF  
INTEGRATED CIRCUIT DESIGNS

ABSTRACT

Method and apparatus for forming timing parameters for a circuit design having a predefined routing topology within an integrated circuit is described. Sets of timing attributes are determined for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the circuit design may be placed. Timing parameters are formed in response to the sets of timing attributes. The timing parameters are then associated with the routing topology.